REMARKS

The claims are claims 1 to 11.

The application has been amended at several locations to correct minor errors.

Claims 1, 6, 7 and 10 are amended. Claims 1, 6 and 7 are amended to overcome the rejection under 35 U.S.C. 112. Claim 10 is amended to change "input operations" to "output operations" to match the recitation of base claim 7.

Claims 1, 6 and 7 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter. The Examiner states that the phrase "determining target state programming bits to set the least input clock delay passing the input operation test" is unclear.

Claims 1, 6 and 7 are amended to present proper language under 35 U.S.C. 112.

As amended claims 1, 6 and 7 recite the determining programming to set clock delay "equal to the delay of said delayed" clock passing all operations. This recitation is proper because the recited setting refers to the delayed clock which passes all operations in a previous paragraph. Accordingly, claims 1, 6 and 7 are proper under 35 U.S.C. 112.

Claims 1, 4, 6, 7 and 10 were rejected under 35 U.S.C. 102(b) as anticipated by Erickson U.S. Patent Application Publication No. 2002/0004926. Paragraph 6 does not list claims 4 and 10 as anticipated by Erickson. However, paragraph 6 recites a rejection of claims 4 and 10 over Erickson.

Claims 1, 6 and 7 recite subject matter not anticipated by Erickson. Claim 1 recites "successive testing data input operation with an incrementally delayed input clock." Claims 6 and 7 recite "successive testing data output operation with an incrementally delayed output clock." The Applicants respectfully submit that Erickson fails to teach the recited successive testing with incrementally delayed signals. Erickson illustrates at Figure 3 simultaneously delaying the delayed data signal from delay 51 in plural delay circuits 74, 75, 76, 77, 78 an 79. Erickson illustrates at Figure 7 simultaneously delaying data signal 14 in plural delay circuits 74, 75, 76, 77, 78 and 79. Thus Erickson teaches simultaneous delays while the claims recite successive testing with incrementally delayed signals. Accordingly, Erickson teaches a parallel process while claims 1, 6 and 7 recite a serial process. Accordingly, claims 1, 6 and 7 are allowable over Erickson.

Claims 1, 6 and 7 recite further subject matter not anticipated by Erickson. Claim 1 recites "until all input operations pass." Claims 6 and 7 recite "until all output operations pass." The Applicants respectfully submit that Erickson fails to teach the recited passing of input or output operations. Erickson states at paragraph [0041]:

> "When the values on connections 63-69 are logically different, the feedback mechanism 92 is designed to transmit a feedback signal on connection 95 to delay mechanism 51."

Erickson states at paragraph [0042]:

> "If the value on connection 66 is different than any of the values on connections 63-65, then the delay mechanism 51, in response to the feedback signal on connection 95, is designed to decrease the delay associated with the delay mechanism 51."

Erickson also states at paragraph [0043]:

> "In addition, if the value on connection 66 is different than any of the values on connections 67-69, then the delay mechanism 51, in response to the feedback signal on connection

> 95, is designed to increase the delay associated with the delay mechanism 51."

The Applicants respectfully submit that none of these "test" results indicates whether "all input operations pass" as required by claim 1 or "all output operations pass" as required by claims 6 and 7. It is apparent that Erickson tests a different thing than recited in claims 1, 6 and 7. Accordingly, claims 1, 6 and 7 are allowable over Erickson.

Claims 1, 6 and 7 recite yet further subject matter not anticipated by Erickson. Claims 1, 6 and 7 recite "writing the target state of programming bits into a write once memory." The Applicants respectfully submit that Erickson fails to teach such a "write once memory." The OFFICE ACTION cites paragraph [0028] of Erickson as anticipating this subject matter. Erickson states in paragraph [0028]:

> "In the context of this document, a "computer-readable medium" can be any means that can contain, store, communicate, propagate, or transport the program for use by or in connection with the instruction execution system, apparatus, or device. The computer readable medium can be, for example but not limited to, an electronic, magnetic, optical, electromagnetic, infrared, or semiconductor system, apparatus, device, or propagation medium. More specific examples (a nonexhaustive list) of the computer-readable medium would include the following: an electrical connection (electronic) having one or more wires, a portable computer diskette (magnetic), a random access memory (RAM) (magnetic), a read-only memory (ROM) (magnetic), an erasable programmable read-only memory (EPROM or Flash memory) (magnetic), an optical fiber (optical), and a portable compact disc read-only memory (CDROM) (optical)."

This extensive list of computer readable memory fails to disclose the recited write once memory. Note that the recited portable computer diskette, random access memory and erasable programmable read-only memory are read/write memories enabling the computer to both read from and write to the memory. The recited read-only memory and portable compact disc read-only memory are read only enabling the computer to read from the memory but prohibiting the computer from writing to the memory. None of these memories are of the type permitting the computer to read from the memory and to write to the memory only once as the recited "write once memory." The above quoted portions of paragraphs [0042] and [0043] tend to indicate that feedback mechanism 92 operates continuously and provides adjustments to the delay of delay mechanism 51 on a continual basis. This teaching of Erickson negates an inference that the extensively listed memory types of paragraph [0028] include the recited "write once memory." The existence of such an extensive list without naming any memories in the class of memories recited in claims 1, 6 and 7 and the implication of continuous adjustment of delay mechanism 51 indicates that "write once memory" was not contemplated by Erickson. Accordingly, claims 1, 6 and 7 are allowable over Erickson.

Claims 4 and 10 recite subject matter not anticipated by Erickson. Claim 4 recites "said step of writing the target state of programming bits into a write once memory includes writing programming bits not related to data input operations performance." Claim 10 recites "said step of writing the target state of programming bits into a write once memory includes writing programming bits not related to data output operations performance." The OFFICE ACTION cites memory 25 illustrated in Figure 3 of Erickson as anticipating this subject matter. The Applicants respectfully submit that Erickson fails to teach the storage of any other programming bits than those related to the data input and output operations. Firstly, claims 4 and 10 recite these programming bits are stored in the write once memory. As noted above, Erickson states in paragraph [0028]:

> "Furthermore, control logic 24 for controlling the features of the signal comparison system 20 can be stored in computer memory 25 of the computer system 23."

Erickson states at paragraph [0047]:

> "Control logic 24 is designed to provide control signals to mulitplexer 105 to instruct multiplexer 105 on which connection 10a, 106b, 106c, 106d or 107 to select."

The above quoted portion of paragraph [0028] is the only mention of computer memory 25 in Erickson. This teaching refers to control logic 24 "for controlling the features of the signal comparison system 20." Erickson also teaches that control logic 24 controls multiplexer 105 which is taught as part of delay mechanism 51. Accordingly, Erickson fails to teach storage of any "programming bits" not related to the data input or data output operations. Accordingly, claims 4 and 10 are allowable over Erickson.

Claims 2, 3, 5, 8, 9 and 11 are allowed.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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